Micro-instructions

Two-Operand Instructions

* MOV
  1. SOURCEout,Yout, NopA, Zin
* ADD
  1. SOURCEout, Yout, ADD, Zin
* ADC
  1. SOURCEout, Yout, ADC, Zin
* SUB (Dest – Src)
  1. SOURCEout, Yout, SUB, Zin
* SBC
  1. SOURCEout, Yout, SBC, Zin
* AND
  1. SOURCEout, Yout, AND, Zin
* OR
  1. SOURCEout, Yout, OR, Zin
* XNOR
  1. SOURCEout, Yout, XNOR, Zin
* CMP
  1. SOURCEout, Yout, SUB,Zin

One-Operand Instruction

* INC
  1. SOURCEout,Yout, IncA, Zin
* DEC
  1. SOURCEout,Yout, DecA, Zin
* CLR
  1. SOURCEout,Yout, Clear, Zin
* INV
  1. SOURCEout,Yout, NotA, Zin
* LSR
  1. SOURCEout,Yout, LSR\_B, Zin
* ROR
  1. SOURCEout,Yout, ROR\_B, Zin
* RRC
  1. SOURCEout,Yout, RRC\_B, Zin
* ASR
  1. SOURCEout,Yout, ASR\_B, Zin
* LSL
  1. SOURCEout,Yout, LSL\_B, Zin
* ROL
  1. SOURCEout,Yout, ROL\_B, Zin
* RLC
  1. SOURCEout,Yout, RLC\_B, Zin

Branching

1. PCout, Yin
2. DecoderOffsetOut, Yout, ADD, Zin
3. Zout, PCin
4. END

JSR

1. PCout, MARin, Rd, IncPc, Yin
2. MDRout, Yout, ADD, Zin, PCincr.in, SPoutDec
3. PCout, MDRin, SPinDec
4. SPout, MARin, Wr
5. Zout, PCin

Interrupt

1. FlagOut, MDRin, SPoutDec
2. SPinDec
3. SPout, MARin, Wr, SPoutDec
4. PCout, MDRin, SPinDec
5. SPout, MARin, Wr
6. IntAddressOut, PCin

IRET

1. SPout, MARin, Rd, SPoutInc
2. MDRout, FlagIn, SPinInc
3. SPout, MARin, Rd, SPoutInc
4. MDRout, PCin, SPinInc

RTS

1. Spout, MARin, Rd, SPoutInc
2. MDRout, PCin, SPinInc

Fetch & Decode

1. PCout, MARin, Rd, IncPc
2. PCin(incrementor), MDRout, IRin

Fetch Source: All—Bit-ORing:

R0out, SOURCEin

R1out, SOURCEin

R2out, SOURCEin

R3out, SOURCEin

R4out, SOURCEin

R5out, SOURCEin

R6out, SOURCEin

R7out, SOURCEin

Register indirect

1. SOURCEout, MARin, Rd
2. MDRout, SOURCEin

Auto Increment:

1. SOURCEout, MARin, Rd, Zin, Inc
2. Bit-ORing:
   * Zout, R0in
   * Zout, R1in
   * Zout, R2in
   * Zout, R3in
   * Zout, R4in
   * Zout, R5in
   * Zout, R6in
   * Zout, R7in

Auto Decrement

1. SOURCEout, Dec, Zin
2. Bit-ORing:
   * Zout, R0in, MARin, Rd
   * Zout, R1in, MARin, Rd
   * Zout, R2in, MARin, Rd
   * Zout, R3in, MARin, Rd
   * Zout, R4in, MARin, Rd
   * Zout, R5in, MARin, Rd
   * Zout, R6in, MARin, Rd
   * Zout, R7in, MARin, Rd

Indexed

1. PCout, MARin, Rd, IncPc
2. MDRout, Yin, PCincr.in
3. SOURCEout, Yout, Add, Zin
4. Zout, MARin, Rd

**Other than Register Direct/Indirect:**

1. Bit-ORing
   * MDRout, MARin, Rd
   * MDRout, SOURCEin

Fetch Destination: All—Bit-ORing:

R0out, DESTin

R1out, DESTin

R2out, DESTin

R3out, DESTin

R4out, DESTin

R5out, DESTin

R6out, DESTin

R7out, DESTin

Register Indirect

1. DESTout, MARin, Rd
2. MDRout, DESTin

Autoincrement

DESTout, MARin,Rd,Inc,Zin

Bit OR on: Zout, R0in

Zout, R1in

Zout, R2in

Zout, R3in

Zout, R4in

Zout, R5in

Zout, R6in

Zout, R7in

Autodecrement

DESTout, Dec, Zin

Bit OR on: Zout, R0in, MARin, Rd

Zout, R1in, MARin, Rd

Zout, R2in, MARin, Rd

Zout, R3in, MARin, Rd

Zout, R4in, MARin, Rd

Zout, R5in, MARin, Rd

Zout, R6in, MARin, Rd

Zout, R7in, MARin, Rd

Indexed

1. PCout, MARin, IncPc, Rd
2. PCin(incrementor), MDRout, Yin
3. DESTout, Yout, Add, Zin
4. Zout, MARin, Rd

Other than Register Direct/Indirect—Bit-ORing

1. MDRout,MARin,Rd
2. MDRout, DESTin

Save in Dest: Register direct—Bit-ORing:

Zout, R0out

Zout, R1out

Zout, R2out

Zout, R3out

Zout, R4out

Zout, R5out

Zout, R6out

Zout, R7out

**Else:** Zout, MDRin, Wr